Microprocessors and Microcontrollers (EE-231)

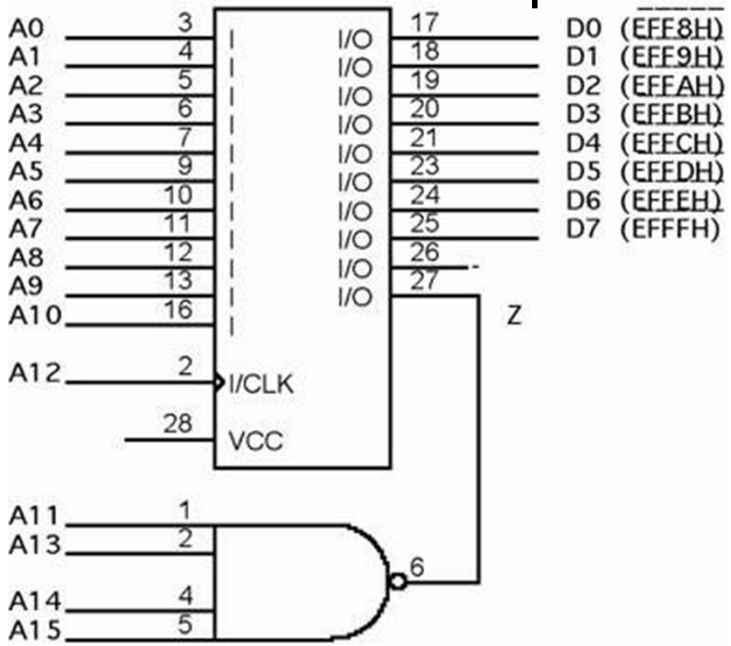
Lecture-13

Main Objectives

- I/O Address Decoding
  - 16-bit address decoding
- 82C55 PPI (Programmable Peripheral Interface)
- 8254 Interval Timer

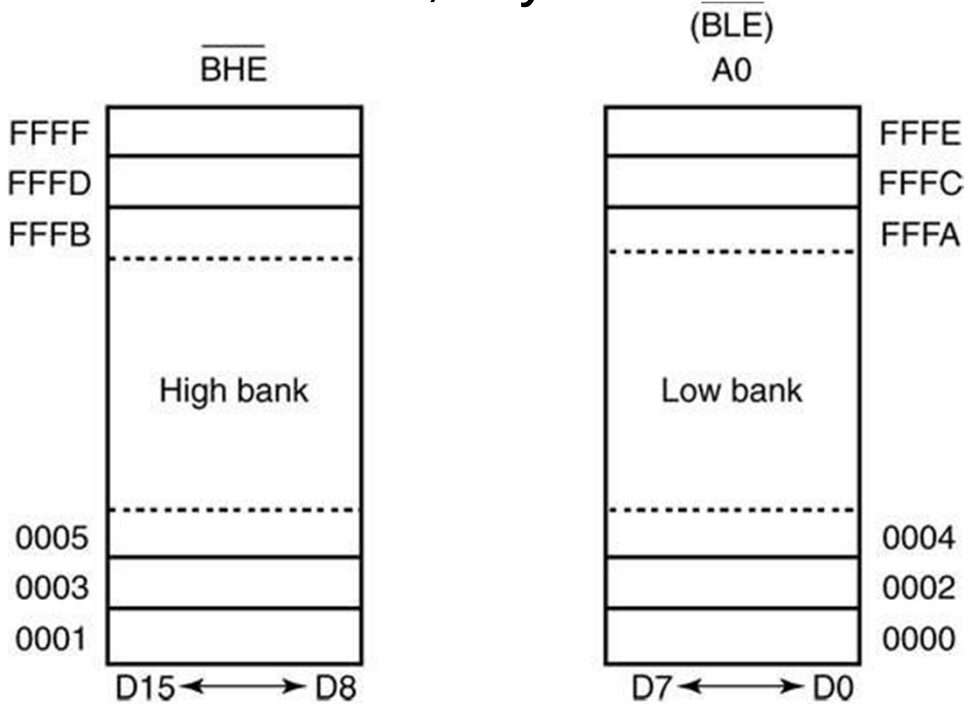
Decoding 16-Bit I/O Port Addresses

- PC systems typically use 16-bit I/O addresses.
- The difference between decoding an 8-bit and a 16-bit I/O address is that eight additional address lines (A_{15}–A_8) must be decoded.
- Figure illustrates a circuit that contains a PLD and a 4-input NAND gate used to decode I/O ports EFF8H–EFFFH.
- PLD generates address strobes for I/O ports



8- and 16-Bit Wide I/O Ports

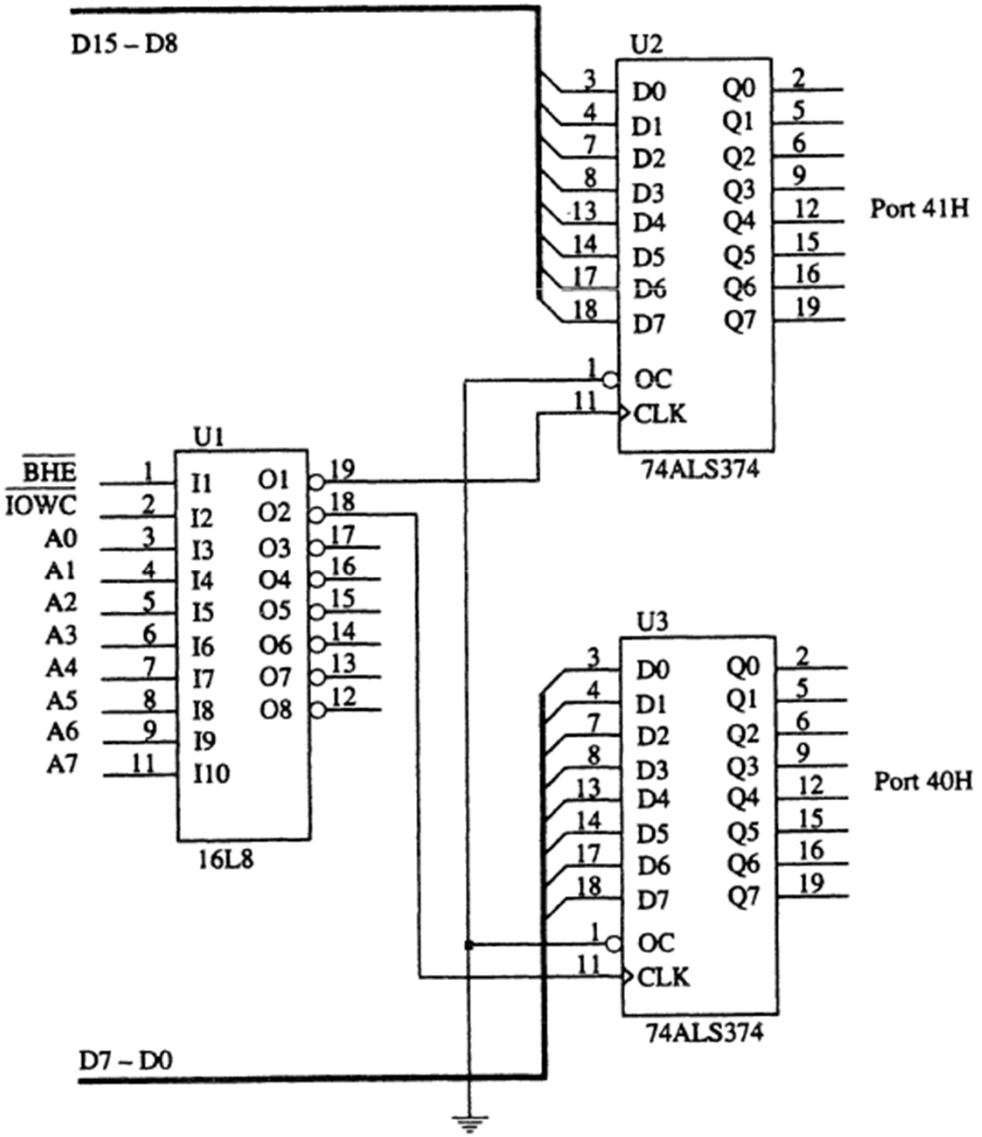
- Data transferred to an 8-bit I/O device exist in one of the I/O banks in a 16-bit processor such as 80386SX.
- The I/O system on such a microprocessor contains two 8-bit memory banks.
- Because two I/O banks exist, any 8-bit I/O write requires a separate write.



8- and 16-Bit Wide I/O Ports

- I/O reads don't require separate strobes.
- Figure (on next page) shows a system with two different 8-bit output devices, located at 40H and 41H.
- These are 8-bit devices and appear in different I/O banks.
  - thus, separate I/O write signals are generated to clock a pair of latches that capture port data

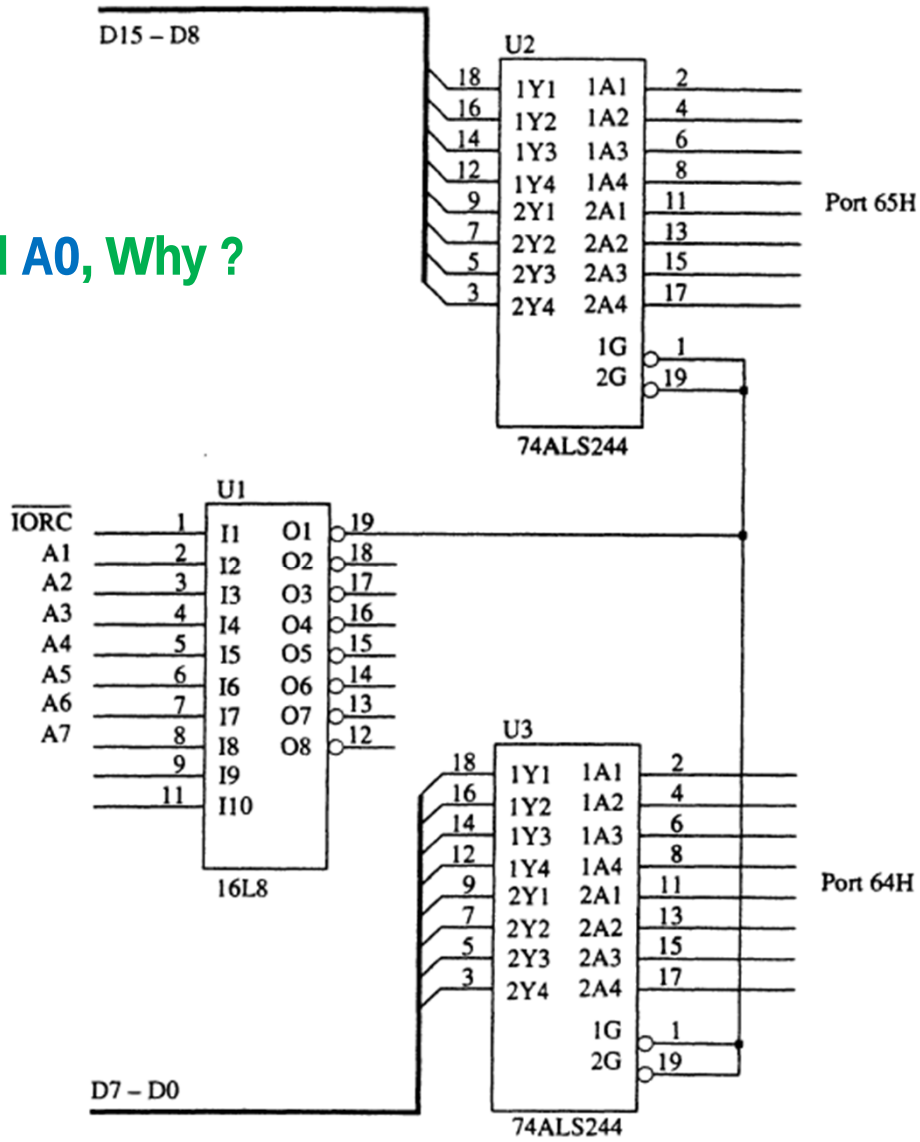
An I/O port decoder that selects ports 40H and 41H for output data.



- all I/O ports use 8-bit addresses
- ports 40H & 41H can be addressed as separate 8-bit ports
- or as one 16-bit port

A 16-bit-wide port decoded at I/O addresses 64H and 65H used as Input device

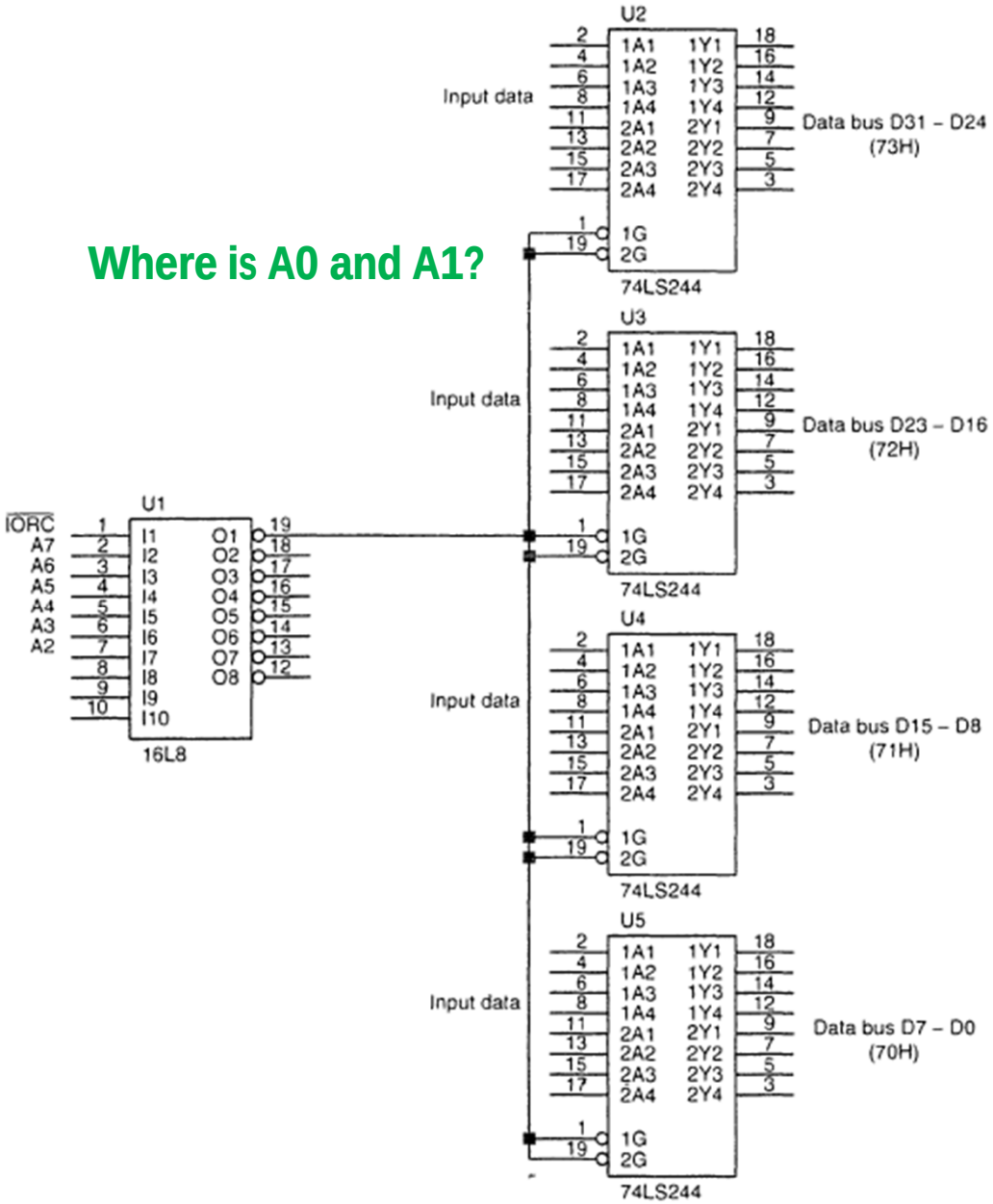
No BHE and A0, Why ?



32-Bit-Wide I/O Ports

- May eventually become common because of newer buses found in computer systems.
- The EISA system bus supports 32-bit I/O as well as the VESA local and current PCI bus.
- Figure shows a 32-bit input port for 80386DX - 80486DX microprocessor.
- The circuit uses a single PLD to decode the I/O ports and four 74HCT244 buffers to connect the I/O data to the data bus.

A 32-bit-wide port decoded at 70H through 73H for the 80486DX microprocessor.



- I/O ports decoded by this interface are the 8-bit ports 70H–73H
- When writing to access this port, it is crucial to use the address 70H for 32-bit input
- as instruction
  IN EAX, 70H

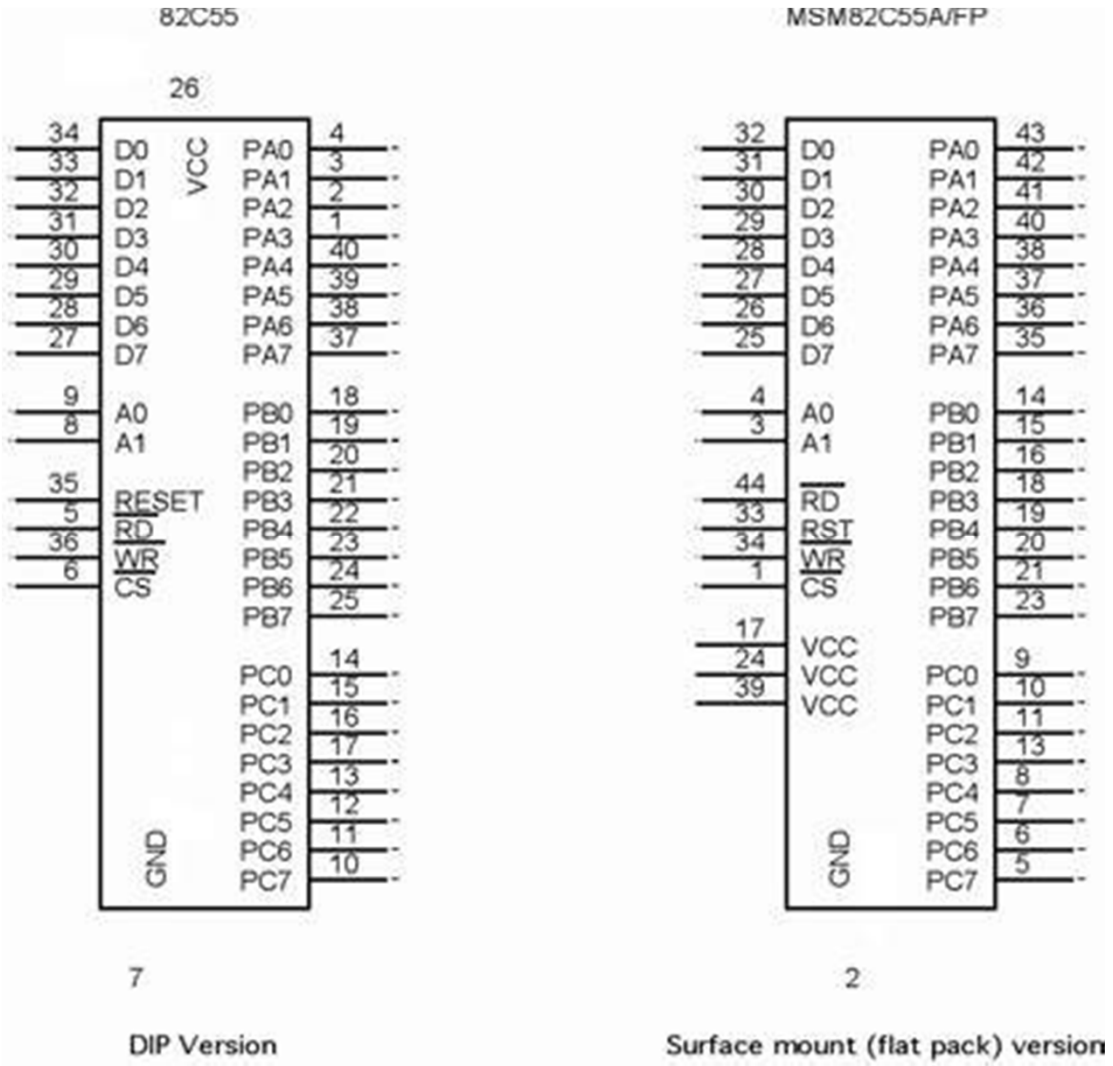
The Programmable Peripheral Interface

- 82C55 **programmable peripheral interface** (PPI) is a popular, low-cost interface component found in many applications.
- The PPI has 24 pins for I/O, programmable in groups of 12 pins and in three distinct modes of operation.
- 82C55 can interface any TTL-compatible I/O device to the microprocessor.
- The 82C55 requires wait states if operated with a processor using higher than an 8 MHz clock.
- Because I/O devices are inherently slow, wait states used during I/O transfers do not impact significantly upon the speed of the system.
- The 82C55 still finds application even in the latest Core2-based computer system.
- 82C55 is used for interface to the keyboard and parallel printer port in many PCs.

Basic Description of the 82C55

- The three I/O ports (labeled A, B, and C) are programmed as groups.
  - group A connections consist of port A (PA_7–PA_0) and the upper half of port C (PC_7–PC_4)
  - group B consists of port B (PB_7–PB_0) and the lower half of port C (PC_3–PC_0)
- 82C55 is selected by its $\overline{CS}$ pin for programming and reading/writing to a port.

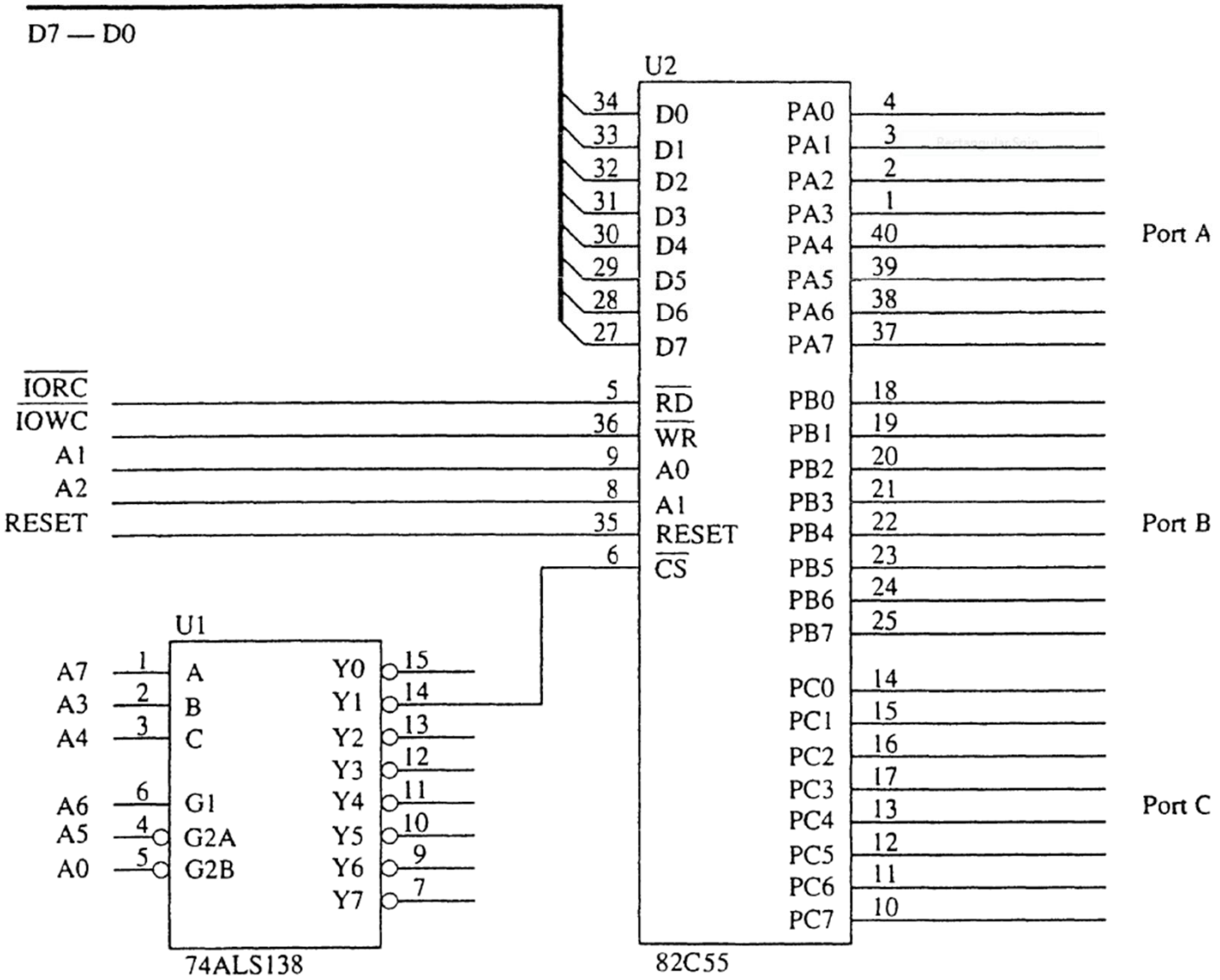
The pin-out of the 82C55



Basic Description of the 82C55

- In the PC, a pair of 82C55s, or equivalents, are decoded at I/O ports 60H–63H and also at ports 378H–37BH.
- For 82C55 to be read or written, the CS input must be logic 0 and the correct I/O address must be applied to the A_1 and A_0 pins.
- Figure(on next slide) shows an 82C55 connected to the 80386SX so it functions at 8-bit addresses C0H (port A), C2H (port B), C4H (port C), and C6H (command register).
  - this interface uses the low bank of the I/O map
- All 82C55 pins are direct connections to the 80386SX, except the CS pin. The pin is decoded/selected by a 74ALS138 decoder.
- A RESET to 82C55 sets up all ports as simple input ports using mode 0 operation.

The 82C55 interfaced to the low bank of the 80386SX microprocessor.



Basic Description of the 82C55

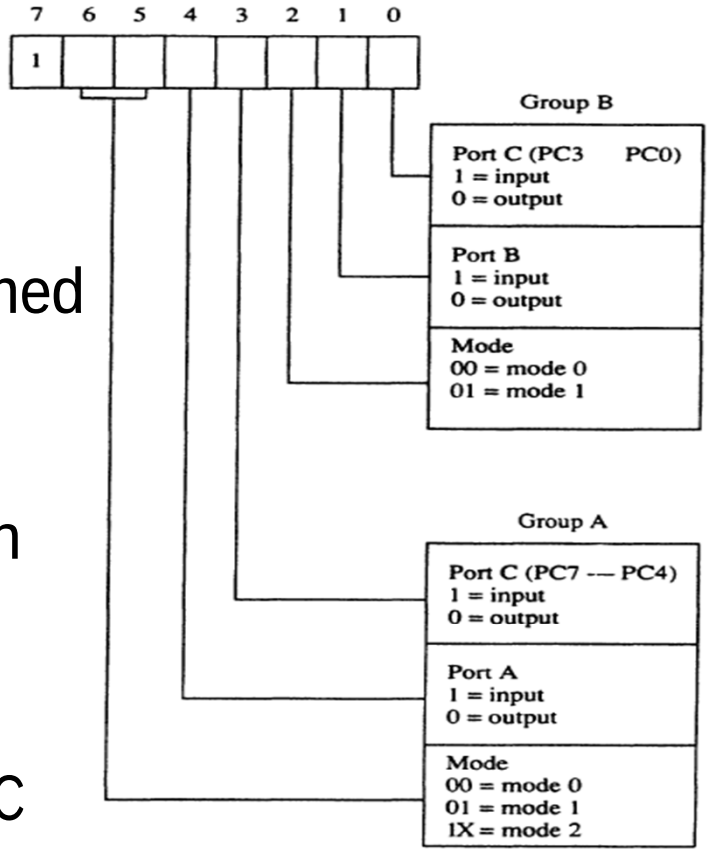
- 82C55 is interfaced to the PC at port addresses 60H–63H for keyboard control.
  - also for controlling the speaker, timer, and other internal devices such as memory expansion
- It is also used for the parallel printer port at I/O ports 378H–37BH.

Programming the 82C55

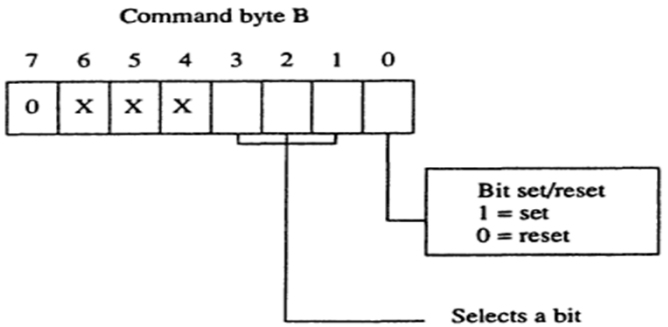
- 82C55 is programmed through two internal command registers shown in Figure.
- Bit position 7 selects either command byte A or command byte B.
  - command byte A programs functions of group A and B
  - byte B sets (1) or resets (0) bits of port C only if the 82C55 is programmed in mode 1 or 2
- Group B (port B and the lower part of port C) are programmed as input or output pins.

The command byte of the command register in the 82C55. (a) Programs ports A, B, and C. (b) Sets or resets the bit indicated in the select a bit field.

- group B operates in mode 0 or mode 1
- mode 0 is basic input/output mode that allows the pins of group B to be programmed as simple input and latched output connections
- Mode 1 operation is the strobed operation for group B connections
- data are transferred through port B
- handshaking signals are provided by port C



(a)



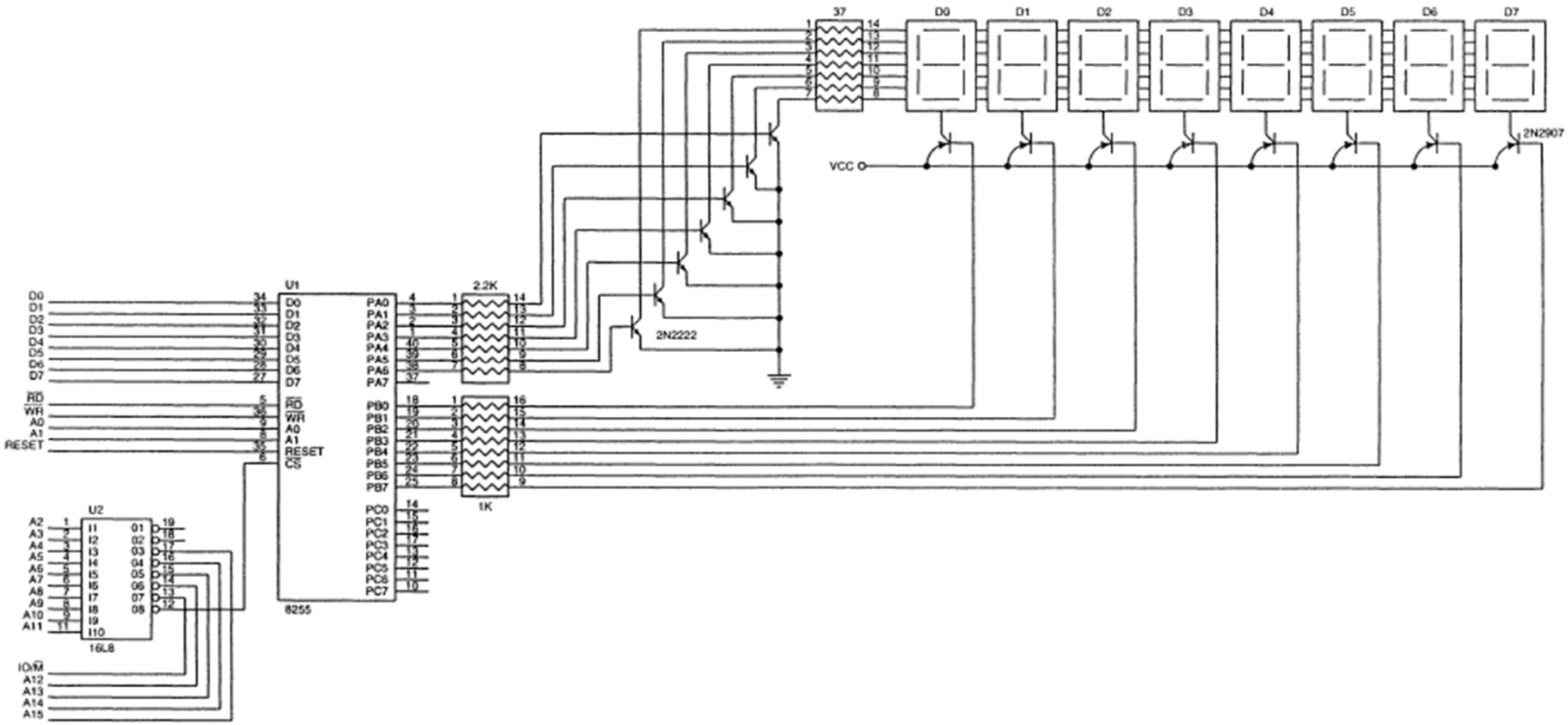
Programming the 82C55

- Group A (port A and the upper part of port C) are programmed as input or output pins.
- Group A can operate in modes 0, 1, and 2.
  - mode 2 operation is a bidirectional mode of operation for port A
- If a 0 is placed in bit position 7 of the command byte, command byte B is selected
- This allows any bit of port C to be set (1) or reset (0), if the 82C55 is operated in either mode 1 or 2.

Mode 0 Operation

- Mode 0 operation causes 82C55 to function:
  - as a buffered input device
  - as a latched output device
- Figure shows 82C55 connected to a set of eight seven-segment LED displays.

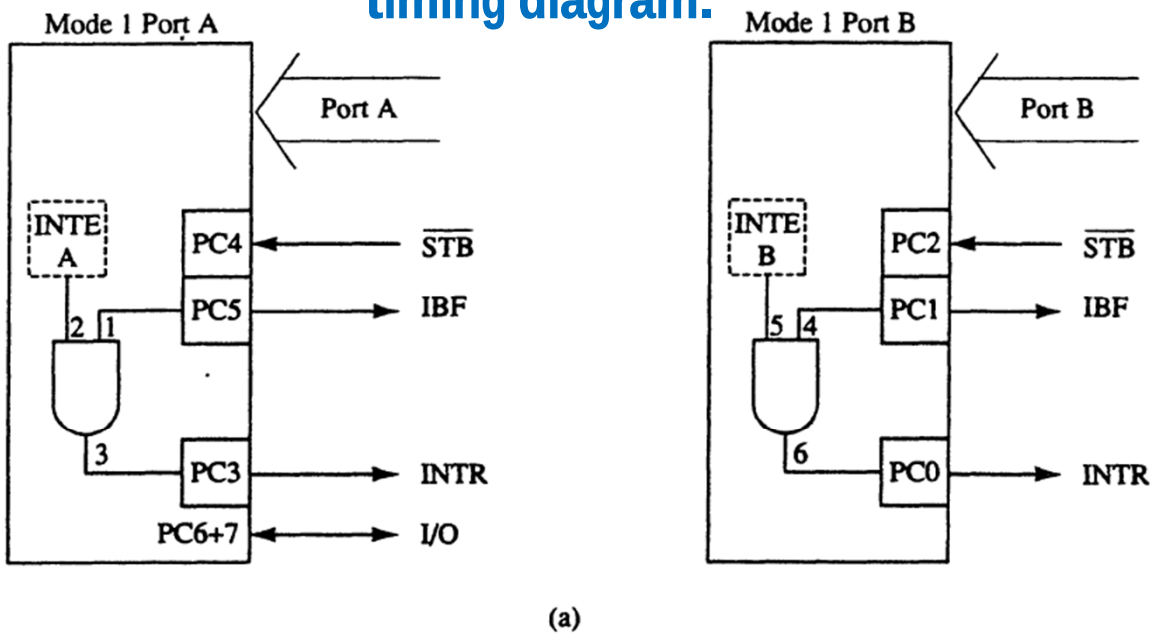
An 8-digit LED display interfaced to the 8088 microprocessor through an 82C55 PIA.



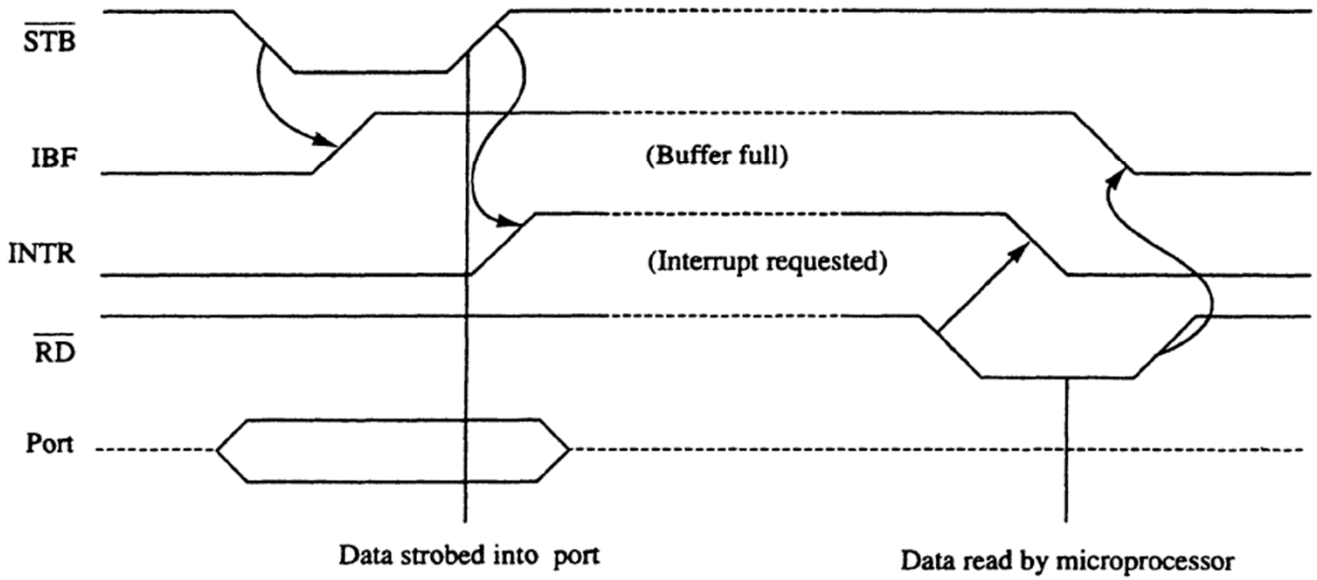
Mode 1 Strobed Input

- Causes port A and/or port B to function as latching input devices.
  - It allows external data to be stored to the port until the microprocessor is ready to retrieve it
- Port C is used in mode 1 operation—not for data, but for control or handshaking signals to help operate either or both port A and B as strobed input ports

Strobed input operation (mode 1) of the 82C55. (a) Internal structure and (b) timing diagram.



(a)



Signal Definitions for Mode 1 Strobed Input

$\overline{\text{STB}}$

The **strobe** input loads data to the port latch, which holds the information until it is input to the microprocessor via the IN instruction.

IBF

Input buffer full is an output indicating that the input latch contains information.

INTR

Interrupt request is an output that requests an interrupt. The INTR pin becomes a logic 1 when STB returns to a logic 1. Cleared when data are input from the port by the processor.

INTE

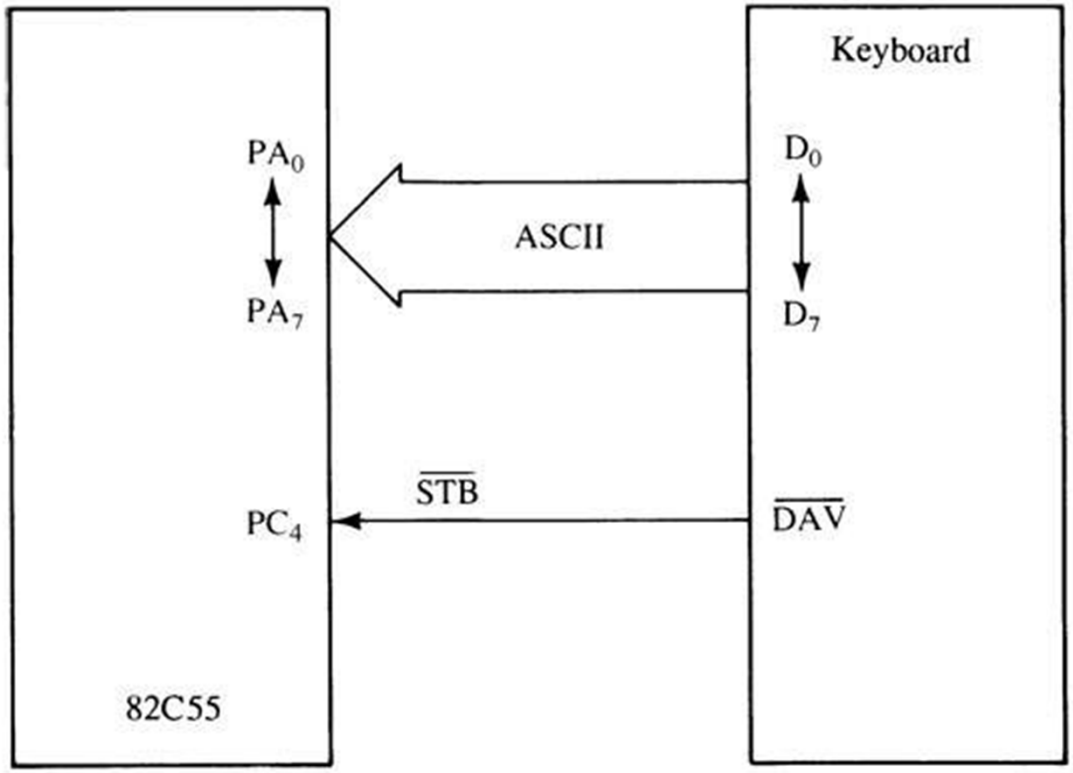
Interrupt enable signal is neither input nor output; it is an internal bit programmed via port PC4 (port A) or PC2 (port B) bit position.

PC7,PC6

The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

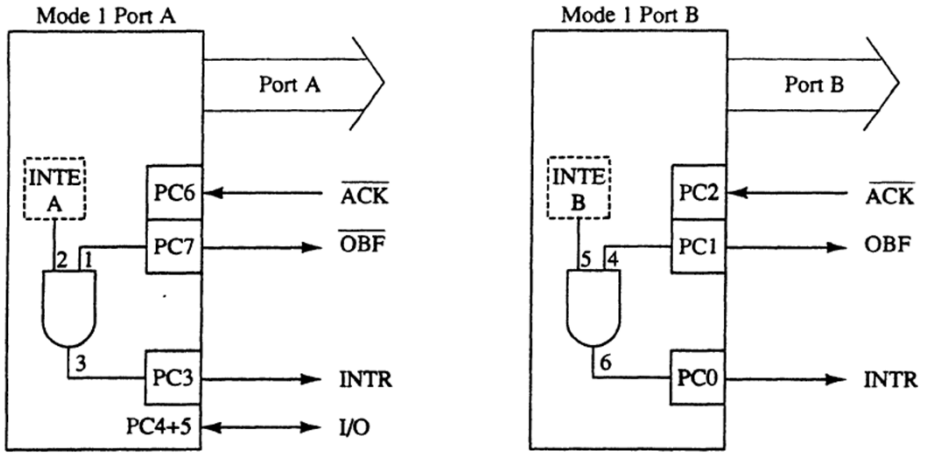
Strobed Input Example

- An example of a strobed input device is a keyboard.
- The keyboard encoder provides a strobe signal whenever a key is depressed.
  - the data output contains ASCII-coded key code

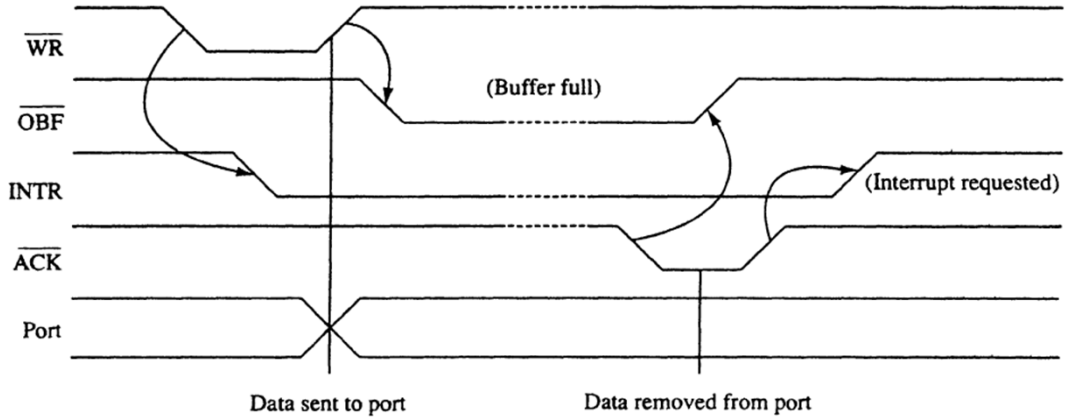


Mode 1 Strobed Output

- When data are written to a strobed output port, the **output buffer full** signal becomes logic 0 to indicate data are present in the port latch.



(a)



Signal Definitions for Mode 1 Strobed Output

$\overline{OBF}$

Output buffer full goes low whenever data are output (OUT) to the port A or B latch. The signal is set to logic 1 when the ACK pulse returns from the external device.

$\overline{ACK}$

The **acknowledge signal** causes the OBF pin to return to logic 1. The ACK signal is a response from an external device, indicating that it has received data from the 82C55 port.

INTE

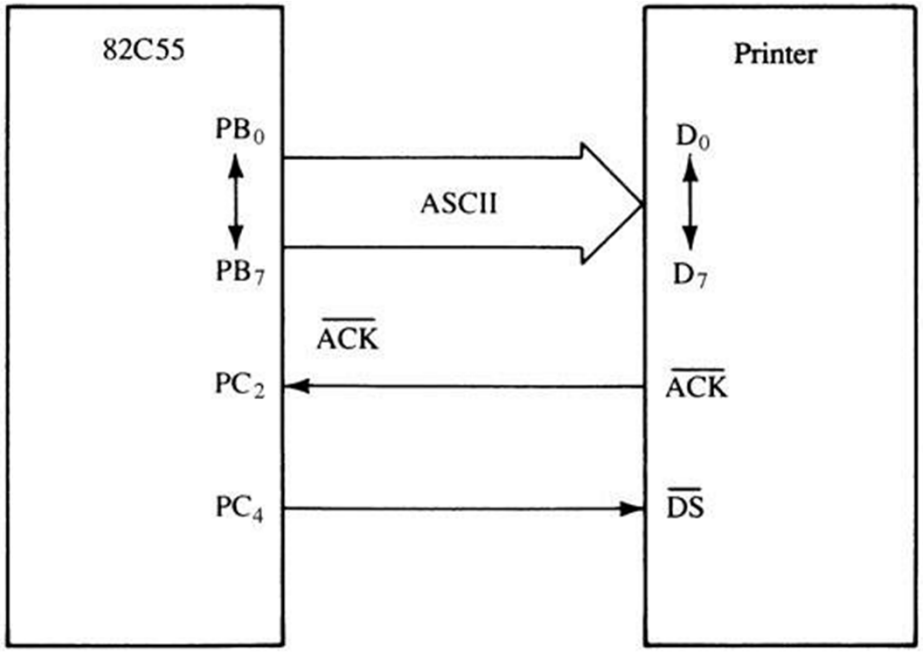
Interrupt enable is neither input nor output; it is an internal bit programmed to enable or disable the INTR pin. INTE A is programmed using PC_6 bit. INTE B is programmed using the PC_2 bit.

PC4,PC5

Port C pins PC4 and PC5 are general-purpose I/O pins.

Strobed Output Example

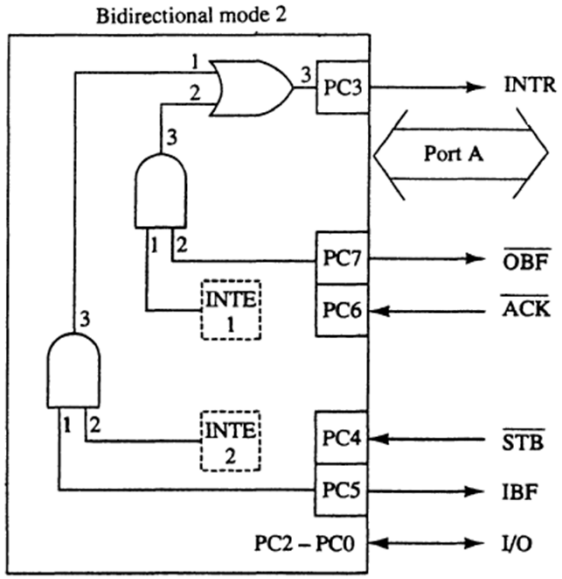
- Its example is printer.
- Figure illustrates port B connected to a parallel printer, with eight data inputs for receiving ASCII-coded data, a $\overline{DS}$ (**data strobe**) input to strobe data into the printer, and an $\overline{ACK}$ output to acknowledge the receipt of the ASCII character.



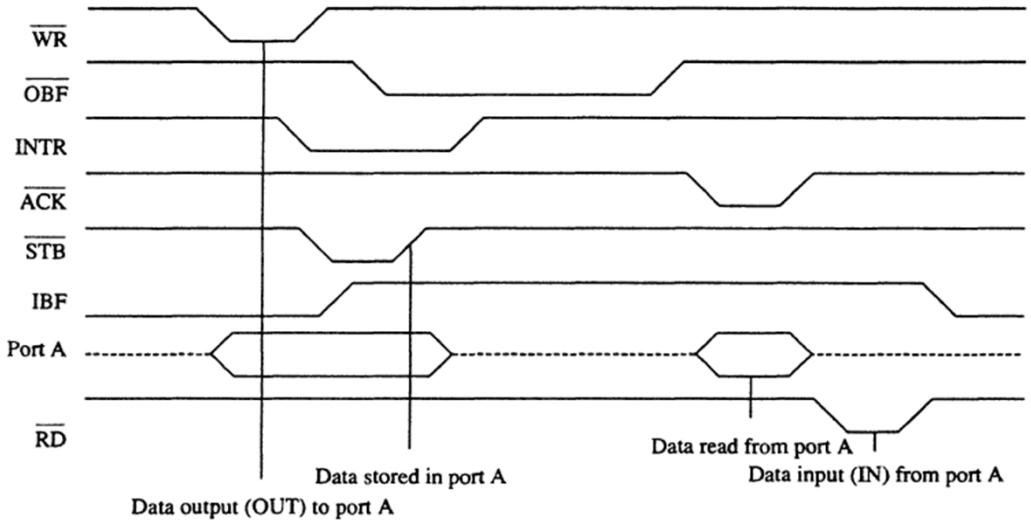
Mode 2 Bidirectional Operation

- Mode 2 is allowed with group A only.
- Port A becomes bidirectional, allowing data transmit/receive over the same eight wires.
  - useful when interfacing two computers
- Also used for IEEE-488 parallel high-speed GPIB (**general- purpose instrumentation bus**) interface standard.
- Figure 11–31 shows internal structure and timing for mode 2 bidirectional operation.

Mode 2 operation of the 82C55. (a) Internal structure and (b) timing diagram.



(a)



Signal Definitions for Bidirectional Mode 2

INTR

Interrupt request is an output used to interrupt the microprocessor for input and output conditions.

$\overline{\text{OBF}}$

Output buffer full is an output indicating the output buffer contains data for the bidirectional bus.

$\overline{\text{ACK}}$

Acknowledge is an input that enables the three-state buffers so that data can appear on port A. If ACK is logic 1, the output buffers of port A are at their high-impedance state.

$\overline{\text{STB}}$

The **strobe** input loads the port A input latch with external data from the bidirectional port A bus.

PC0,1,2

These pins are general-purpose I/O pins in mode 2 controlled by the bit set and reset command.

Signal Definitions for Bidirectional Mode 2

IBF

Input buffer full is an output used to signal that the input buffer contains data for the external bidirectional bus.

$\overline{\text{OBF}}$

Output buffer full is an output indicating the output buffer contains data for the bidirectional bus.

INTE

Interrupt enable are internal bits (INTE1 & INTE2) that enable the INTR pin. The state of the INTR pin is controlled through port C bits PC6 (INTE1) and PC4 (INTE2).

The Bidirectional Bus

- The bidirectional bus is used by referencing port A with the IN and OUT instructions.
- To transmit data through the bidirectional bus, the program first tests to determine whether the output buffer is empty.
  - if so, data are sent to the output buffer via OUT
- The external circuitry also monitors the signal to decide whether the microprocessor has sent data to the bus.

The Bidirectional Bus

- To receive data through the bidirectional port A bus, IBF is tested with software to decide whether data have been strobed into the port.
  - if IBF = 1, data is input using IN
- The external interface sends data to the port by using the $\overline{\text{STB}}$ signal.
  - the IBF signal becomes logic 1 and data at port A are held inside the port in a latch
- When the IN executes, the IBF bit is cleared and data in the port are moved into AL.

82C55 Mode Summary

- Figure shows a graphical summary of the three modes of 82C55.
- Mode 0 provides simple I/O.
- Mode 1 provides strobed I/O.
- Mode 2 provides bidirectional I/O.
- These modes are selected through the command register of the 82C55.

		Mode 0		Mode 1		Mode 2
Port A		IN	OUT	IN	OUT	I/O
Port B		IN	OUT	IN	OUT	Not used
Port C	0	IN	OUT	$INTR_B$	$INTR_B$	I/O
	1			IBF_B	$\overline{OBF}_B$	I/O
	2			$\overline{STB}_B$	$\overline{ACK}_B$	I/O
	3			$INTR_A$	$INTR_A$	INTR
	4			$\overline{STB}_A$	I/O	$\overline{STB}$
	5			IBF_A	I/O	IBF
	6			I/O	$\overline{ACK}_A$	$\overline{ACK}$
	7			I/O	$\overline{OBF}_A$	$\overline{OBF}$

8254 Programmable Interval Timer

- The 8254 consists of three independent 16-bit programmable counters (**timers**).
- Each counter is capable of counting in binary or binary-coded decimal (BCD).
  - maximum allowable input frequency to any counter is 10 MHz
- Useful where the microprocessor must control real-time events.
- Usage includes real-time clocks, event counters, and motor speed/direction control.

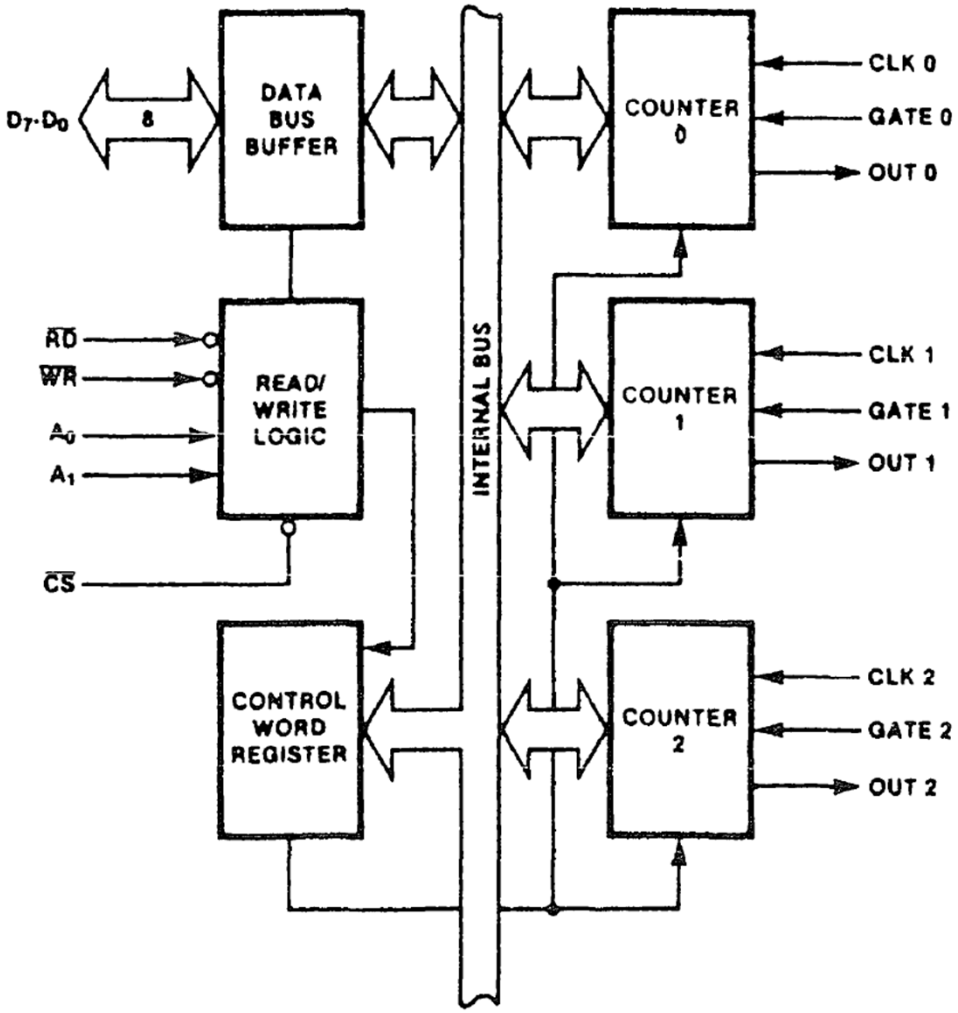
8254 Programmable Interval Timer

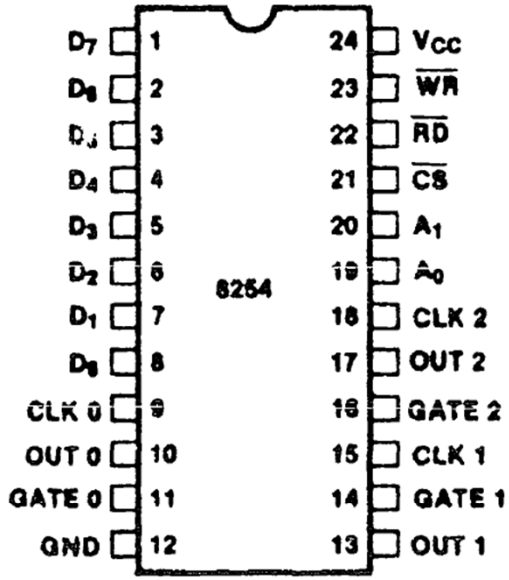
- Timer appears in the PC decoded at ports 40H–43H to do the following:
  1. Generate a basic timer interrupt that occurs at approximately 18.2 Hz
  2. Cause the DRAM memory system to be refreshed
  3. Provide a timing source to the internal speaker and other devices.
- Timer in the PC is an 8253 instead of 8254.

8254 Functional Description

- Figure shows the pin-out of the 8254, a higher-speed version of the 8253, and a diagram of one of the three counters.
- Each timer contains:
  - a CLK input which provides the basic operating frequency to the timer
  - a gate input pin which controls the timer in some modes
  - an output (OUT) connection to obtain the output of the timer

The 8254 programmable interval timer. (a) Internal structure and (b) pin-out. (Courtesy of Intel Corporation.)





8254 Functional Description

- The signals that connect to the processor are the data bus pins (D_7–D_0), $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and address inputs A_1 and A_0.
- Address inputs are present to select any of the four internal registers.
  - used for programming, reading, or writing to a counter
- Timer zero generates an 18.2 Hz signal that interrupts the microprocessor at interrupt vector 8 for a clock tick.
  - often used to time programs and events in DOS
- Timer 1 is programmed for 15 μs, used on the PC to request a DMA action used to refresh the dynamic RAM.
- Timer 2 is programmed to generate a tone on the PC speaker.

Pin Definitions for 8254

A_0, A_1

The address inputs select one of four internal registers within the 8254.

CLK

The **clock** input is the timing source for each of the internal counters. This input is often connected to the PCLK signal from the microprocessor system bus controller.

G

The gate input controls the operation of the counter in some modes of operation

OUT

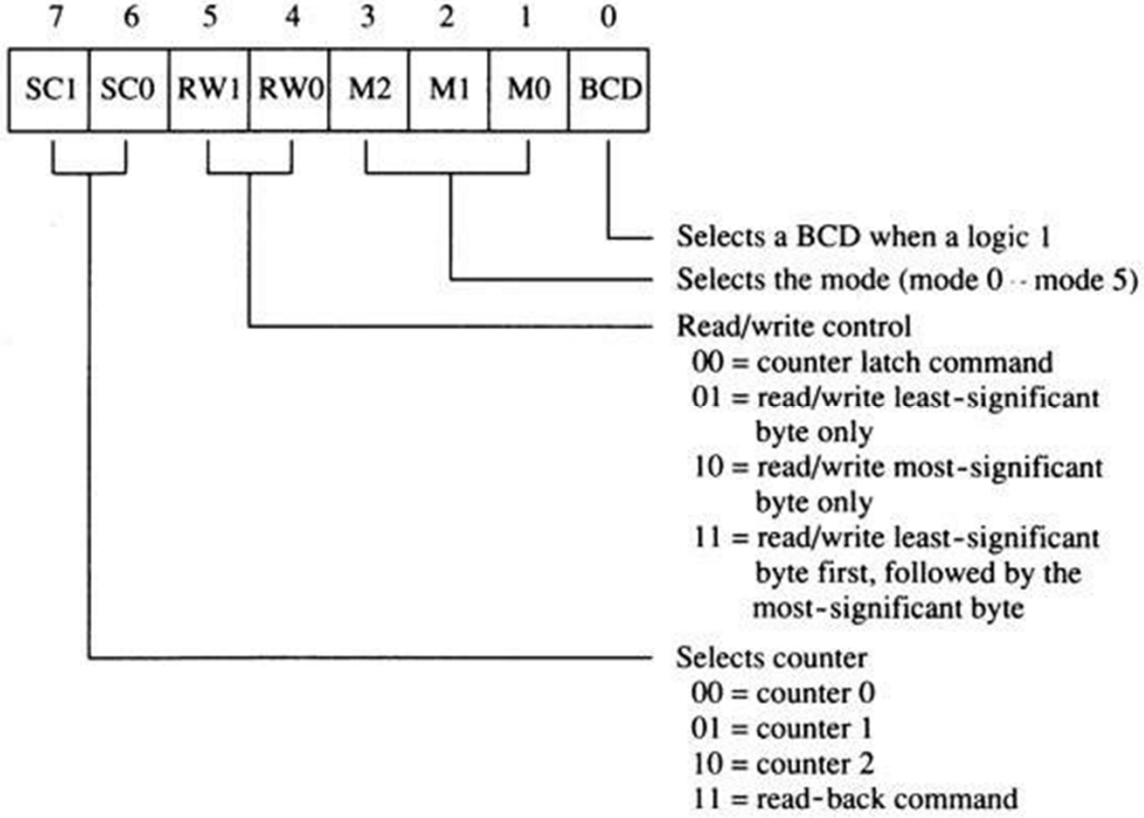
A counter output is where the waveform generated by the timer is available.

$\overline{RD}$,$\overline{WR}$

RD,WR used for reading and writing to or from 8254

Programming the 8254

- Each counter is programmed by writing control word and then the initial count.
- The control word allows the programmer to select the counter, mode of operation, and type of operation (read/write).
  - also selects either a binary or BCD count



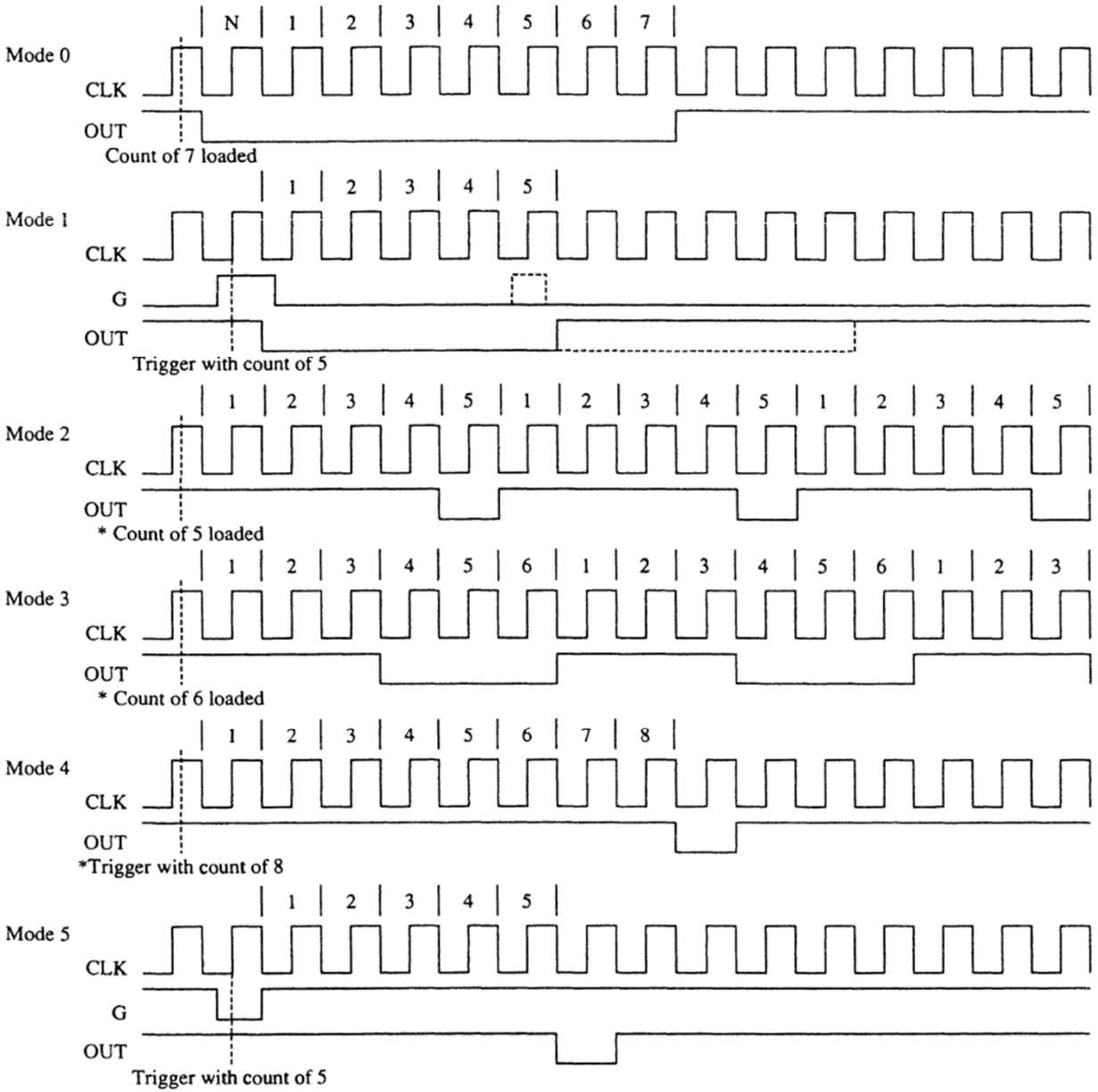
Programming the 8254

- Each counter may be programmed with a count of 1 to FFFFH; A count of 0 is equal
  to FFFFH+I (65,536) or 10,000 in BCD.
- Timer 0 is used in the PC with a divide-by count of 64K (FFFFH) to generate the
  18.2 Hz (18.196 Hz) interrupt clock tick.
  - timer 0 has a clock input frequency of 4.77 MHz + 4 or 1.1925 MHz
- The order of programming is important for each counter, but programming of different counters may be interleaved for better control.

Modes of Operation

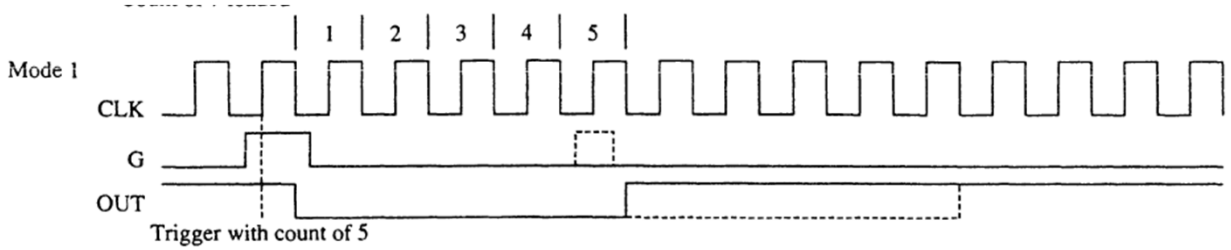
- six modes (0–5) are available to each of the 8254 counters
- each mode functions with the CLK input, the gate (G) control signal, and OUT signal
- **Mode 0**
- Allows 8254 to be used as an events counter.
- Output becomes logic 0 when the control word is written and remains until N plus the number of programmed counts.
- Note that gate (G) input must be logic 1 to allow the counter to count.
- If G becomes logic 0 in the middle of the count, the counter will stop until G again becomes logic 1.

The six modes of operation for the 8254-2 programmable interval timer. The G input stops the count when 0 in modes 2, 3, and 4.



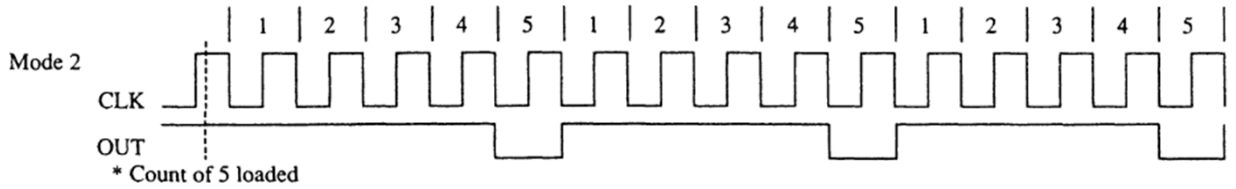
Modes of Operation

- **Mode 1**
- Causes function as a retriggerable, monostable multivibrator (one-shot).
- G input triggers the counter so it develops a pulse at the OUT connection that becomes logic 0 for the duration of the count.
  - if the count is 10, the OUT connection goes low for 10 clocking periods when triggered
- If G input occurs within the output pulse, the counter is reloaded and the OUT connection continues for the total length of the count.



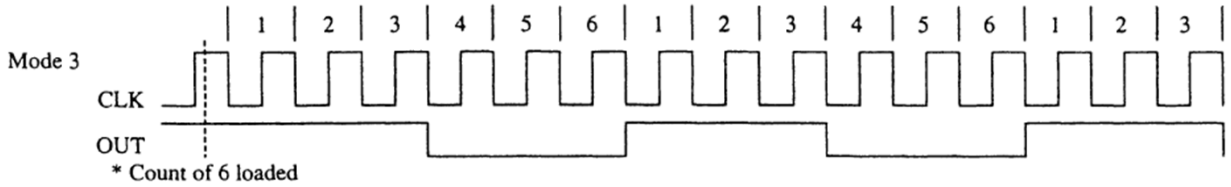
Modes of Operation

- **Mode 2**
- Allows the counter to generate a series of continuous pulses one clock pulse wide.
  - pulse separation is determined by the count
- For a count of 10, output is logic 1 for nine clock periods and low for one clock period.
- The cycle is repeated until the counter is programmed with a new count or until the G pin is placed at logic 0.
  - G input must be logic 1 for this mode to generate a continuous series of pulses



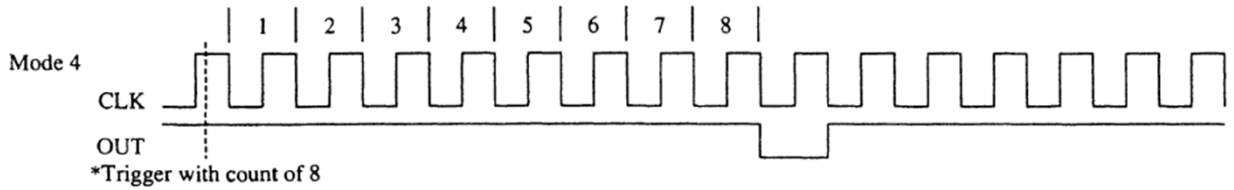
Modes of Operation

- **Mode 3**
- Generates a continuous square wave at the OUT connection, provided the G pin is logic 1.
- If the count is even, output is high for one half of the count and low for one half of the count.
- If the count is odd, output is high for one clocking period longer than it is low.
  - if the counter is programmed for a count of 5, the output is high for three clocks and low for two clocks



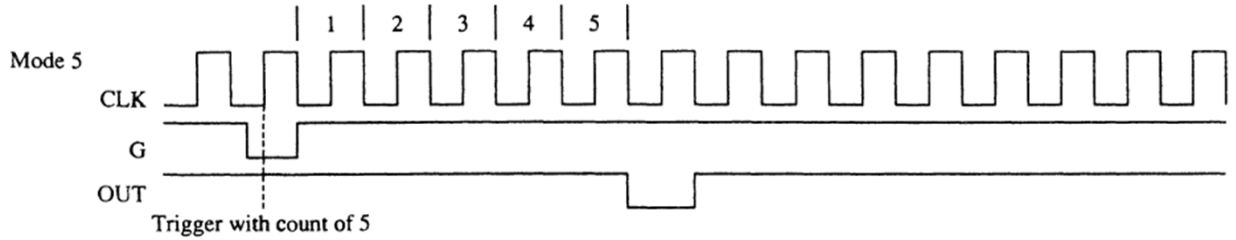
Modes of Operation

- **Mode 4**
- Allows a single pulse at the output.
- If count is programmed as 10, output is high for 10 clocking periods and low for one period.
  - the cycle does not begin until the counter is loaded with its complete count
- Operates as a software triggered one-shot.
- G input must be logic 1 for the counter to operate for these three modes



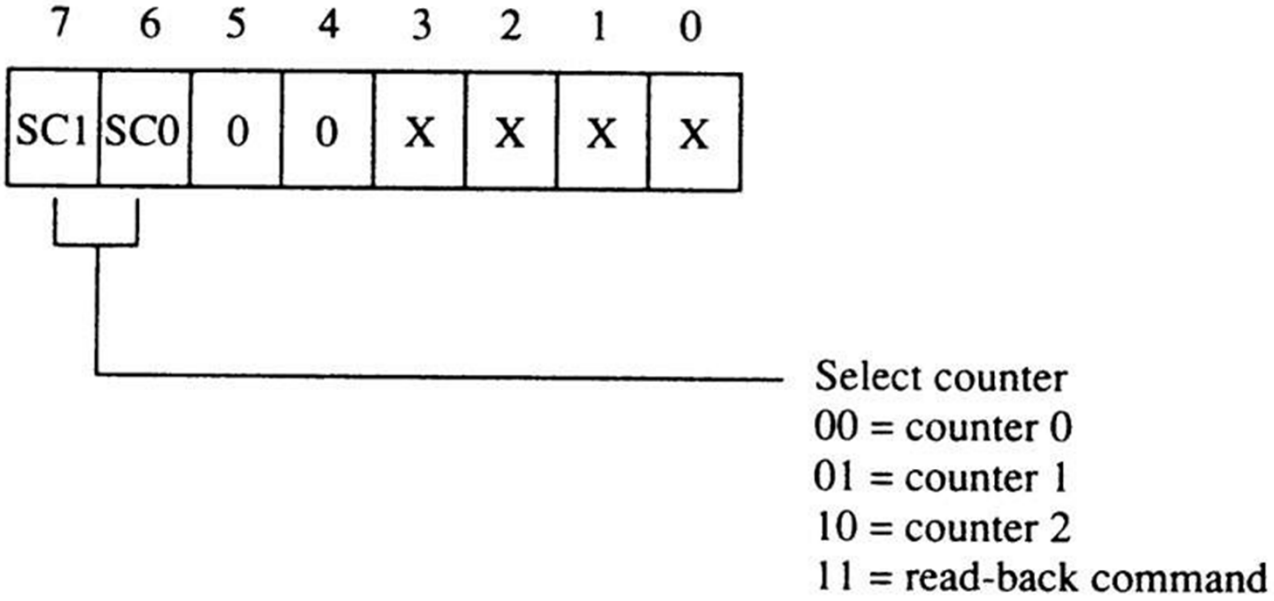
Modes of Operation

- **Mode 5**
- A hardware triggered one-shot that functions as mode 4.
  - except it is started by a trigger pulse on the G pin instead of by software
- This mode is also similar to mode 1 because it is retriggerable.



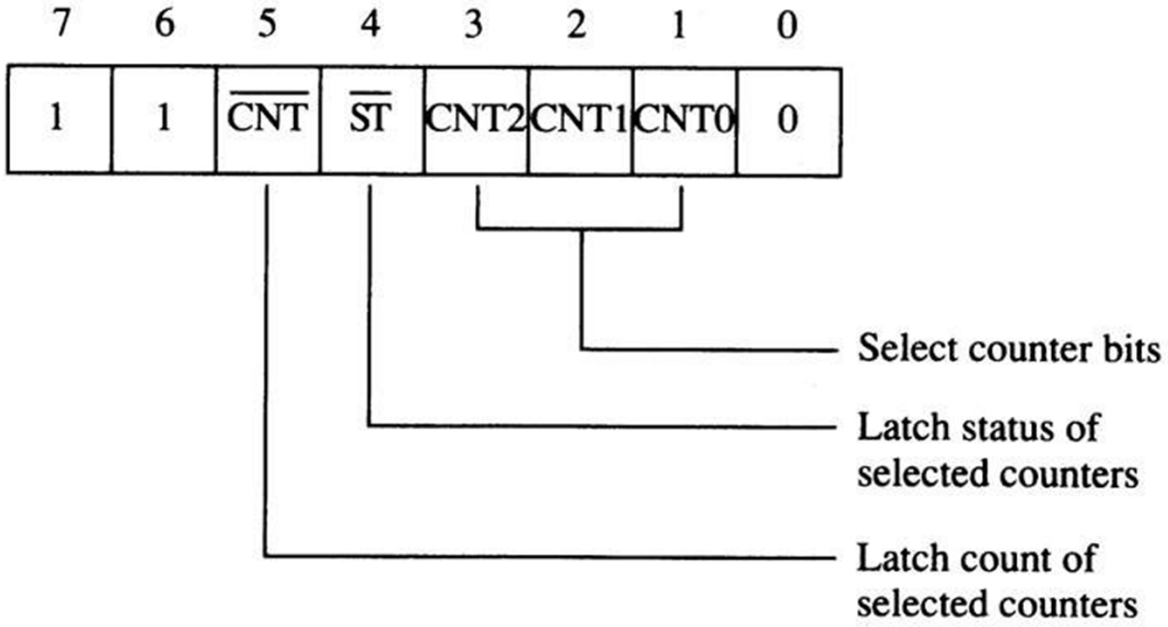
Reading a Counter

- Each counter has an internal latch read with the read counter port operation.
  - the latches will normally follow the count
- If counter contents are needed, the latch can remember the count by programming the counter latch control word.



Reading a Counter

- When a read from the latch or counter is programmed, the latch tracks the contents.
- When necessary for contents of more than one counter to be read at the same time, the read-back control word is used



Reading a Counter

- With the read-back control word, the CNT bit is logic 0 to cause the counters selected by CNT0, CNT1, and CNT2 to be latched.
- If the status register is to be latched, then the bit is placed at logic 0.
- Figure shows the status register, which shows:
  - the state of the output pin
  - whether the counter is at its null state (0)
  - how the counter is programmed

The 8254-2 status register.